WHAT IS CLAIMED IS:

1. An apparatus comprising:

a converter circuit having a dynamic logic input and configured to generate a static logic output on an output node responsive to the dynamic logic input; and

a noise suppression circuit coupled to receive a clock signal and coupled to the output node, wherein a precharge of a dynamic logic circuit generating the dynamic logic input occurs responsive to a first phase of the clock signal, and wherein the noise suppression circuit is configured to actively drive the static logic output on the output node responsive to the first phase.

2. The apparatus as recited in claim 1 wherein the converter circuit is coupled to receive the clock signal and to generate the static logic output further responsive to the clock signal.

3. The apparatus as recited in claim 2 wherein the converter circuit is coupled to receive a plurality of dynamic logic inputs including the dynamic logic input, and wherein the static logic output is a logical combination of the plurality of dynamic logic inputs.

4. The apparatus as recited in claim 1 wherein the noise suppression circuit is coupled to the converter circuit, and wherein the noise suppression circuit is configured to actively drive the static logic output through one or more transistors in the converter circuit.

5. The apparatus as recited in claim 1 wherein the noise suppression circuit is coupled to receive a feedback signal corresponding to the static logic output, wherein the noise suppression circuit is configured to actively drive the static logic output further responsive to the feedback signal.

6. The apparatus as recited in claim 5 further comprising an inverter coupled to the output node and to provide the feedback signal.

7. The apparatus as recited in claim 5 wherein the noise suppression circuit comprises a tristate inverter circuit coupled to receive the feedback signal and coupled to the output node, wherein a tristate control of the tristate inverter circuit is controlled by the clock signal.

8. The apparatus as recited in claim 5 wherein the noise suppression circuit comprises:

a first transistor having a first node, a second node, and a first control node, wherein the first node is coupled to a power supply and the first control node is coupled to receive the feedback signal; and

a second transistor having a third node connected to the second node, a fourth node connected to the output node, and a second control node controlled by the clock signal.

9. The apparatus as recited in claim 8 wherein the noise suppression circuit further comprises a third transistor having a fifth node coupled to ground, a sixth node, and a third control node controlled by the clock signal, wherein the sixth node is coupled to the converter circuit to actively drive the output node through one or more transistors in the converter circuit.

10. The apparatus as recited in claim 8 wherein a size of the first transistor and the second transistor is between about 30%-50% of a size of transistors in the converter circuit.

11. The apparatus as recited in claim 8 wherein a size of the first transistor and the

second transistor is about 30% of a size of transistor in the converter circuit.

12. The apparatus as recited in claim 8 wherein a size of the first transistor and the second transistor is selected according to an expected noise on the output node.

13. A circuit for actively driving an output node on which a static logic signal corresponding to a dynamic logic signal is supplied via a converter circuit, the circuit comprising:

a first transistor having a first node, a second node, and a first control node, wherein the first node is coupled to a power supply and the first control node is coupled to receive a feedback signal corresponding to the static logic signal; and

a second transistor having a third node connected to the second node, a fourth node connected to the output node, and a second control node controlled by the clock signal, wherein a precharge of a dynamic logic circuit generating the dynamic logic input occurs responsive to a first phase of the clock signal, and wherein the second transistor activates during the first phase responsive to the clock signal.

14. The circuit as recited in claim 13 further comprising a third transistor having a fifth node coupled to ground, a sixth node, and a third control node controlled by the clock signal, wherein the sixth node is coupled to the converter circuit to form a current path with at least a fourth transistor in the converter circuit which is coupled to receive the dynamic logic input on its control node.

15. The circuit as recited in claim 14 wherein the first and second transistors are PMOS transistors and the third transistor is an NMOS transistor.

16. The circuit as recited in claim 14 wherein the converter circuit is coupled to receive a plurality of dynamic logic inputs including the dynamic logic input, and wherein the converter circuit includes a plurality of transistors including the fourth transistor, each of the plurality of transistors coupled to receive a respective dynamic logic input of the plurality of dynamic logic inputs on its control node, and wherein the third transistor is coupled in series with the plurality of transistors.

17. The circuit as recited in claim 16 wherein the plurality of transistors are coupled in parallel with each other.

18. The circuit as recited in claim 16 wherein the plurality of transistors are coupled in series with each other.

19. A method comprising:

generating a static logic output on a node responsive to a dynamic logic input; and

actively driving the static logic output on the node responsive to a first phase of a clock signal, wherein a precharge of a dynamic logic circuit generating the dynamic logic input occurs responsive to a first phase of the clock signal.

20. The method as recited in claim 19 wherein the actively driving is further responsive to a feedback signal corresponding to the static logic output.

21. A computer accessible medium comprising one or more data structures representing one or more of:

a converter circuit having a dynamic logic input and configured to generate a static logic output on an output node responsive to the dynamic logic input; and

a noise suppression circuit coupled to receive a clock signal and coupled to the

output node, wherein a precharge of a dynamic logic circuit generating the dynamic logic input occurs responsive to a first phase of the clock signal, and wherein the noise suppression circuit is configured to actively drive the static logic output on the output node responsive to the first phase.